2123 #3 BT

Patent 01.29.03

Docket No.: CYPR-CD00183

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	01/15/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Warren Snyder

Serial No.: 09/975,104 Group Art Unit:

Filed: 10/10/01 Examiner:

Title: CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING FPGA FOR IN-CIRCUIT EMULATION

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..X.. Information Disclosure statement (2 sheets)
..... Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References
..X.. Other: Related Pending US Patent Applications

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$0.00
Other:					$0.00
Total Fees					$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 1/15/2007

By: _____
Anthony C. Murabito
Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00183

Inventor(s): Warren Snyder

Serial No.: 09/975,104 Group Art Unit:

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Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93

The Examiner's attention is respectfully directed to the following related pending U.S. Patent Applications:

CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE";10/10/01; 09/975,115; Snyder et al.

CYPR-CD00184; "HOST TO FPGA INTERFACE IN AN IN-CIRCUIT EMUALTION SYSTEM"; 10/10/01; 09/975,105; Nemecek

CYPR-CD00185; "EMULATOR CHIP-BOARD ARCHITECTURE AND INTERFACE"; 10/1/01; 09/975,030; Snyder et al.

CYPR-CD00186" METHOD FOR BREAKING EXECUTION OF TEST CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS"; 10/10/01; 09/975,338; Nemecek et al.

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(408) 938-9060

Respectfully submitted,

Date: 1/15/2003

By: _____
Anthony C. Murabito
Reg. No. 35,295

Attorney Docket No.: CYPR-CD00183

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Warren Snyder

Serial No.: 09/975,104 Group Art Unit:

Filed: 10/10/01 Examiner:

Title: CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING FPGA FOR IN-CIRCUIT EMULATION

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
	C						
	D						
	E						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	F							
	G							
	H							

Related Pending US Patent Applications

Examiner Initial	No.	Docket Number, Title, Filing Date, Serial Number & Inventors
	I	CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE";10/10/01; 09/975,115; Snyder et al.
	J	CYPR-CD00184; "HOST TO FPGA INTERFACE IN AN IN-CIRCUIT EMUALTION SYSTEM"; 10/10/01; 09/975,105; Nemecek
	K	CYPR-CD00185; "EMULATOR CHIP-BOARD ARCHITECTURE AND INTERFACE"; 10/1/01; 09/975,030; Snyder et al.
	L	CYPR-CD00186" METHOD FOR BREAKING EXECUTION OF TEST CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS"; 10/10/01; 09/975,338; Nemecek et al.

Examiner	Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.